

BG5CT_STB_RDK Main Board Schematics

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Overview

This is the Set Top Box(STB)
Reference Design Main Board Schematic
for Marvell 88DE3288(BG5-CT) High
Definition Media Processor System on Chip

Contents

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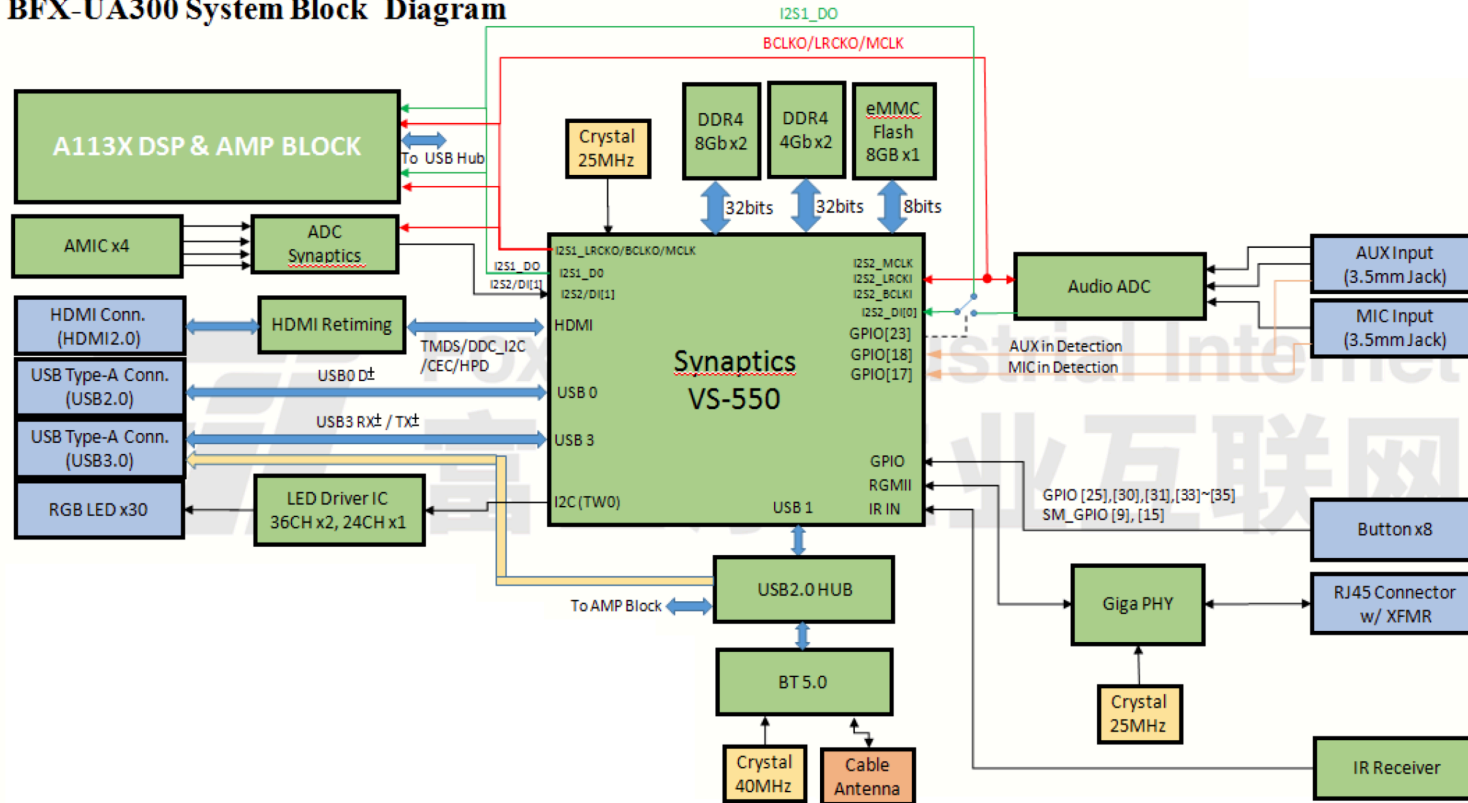
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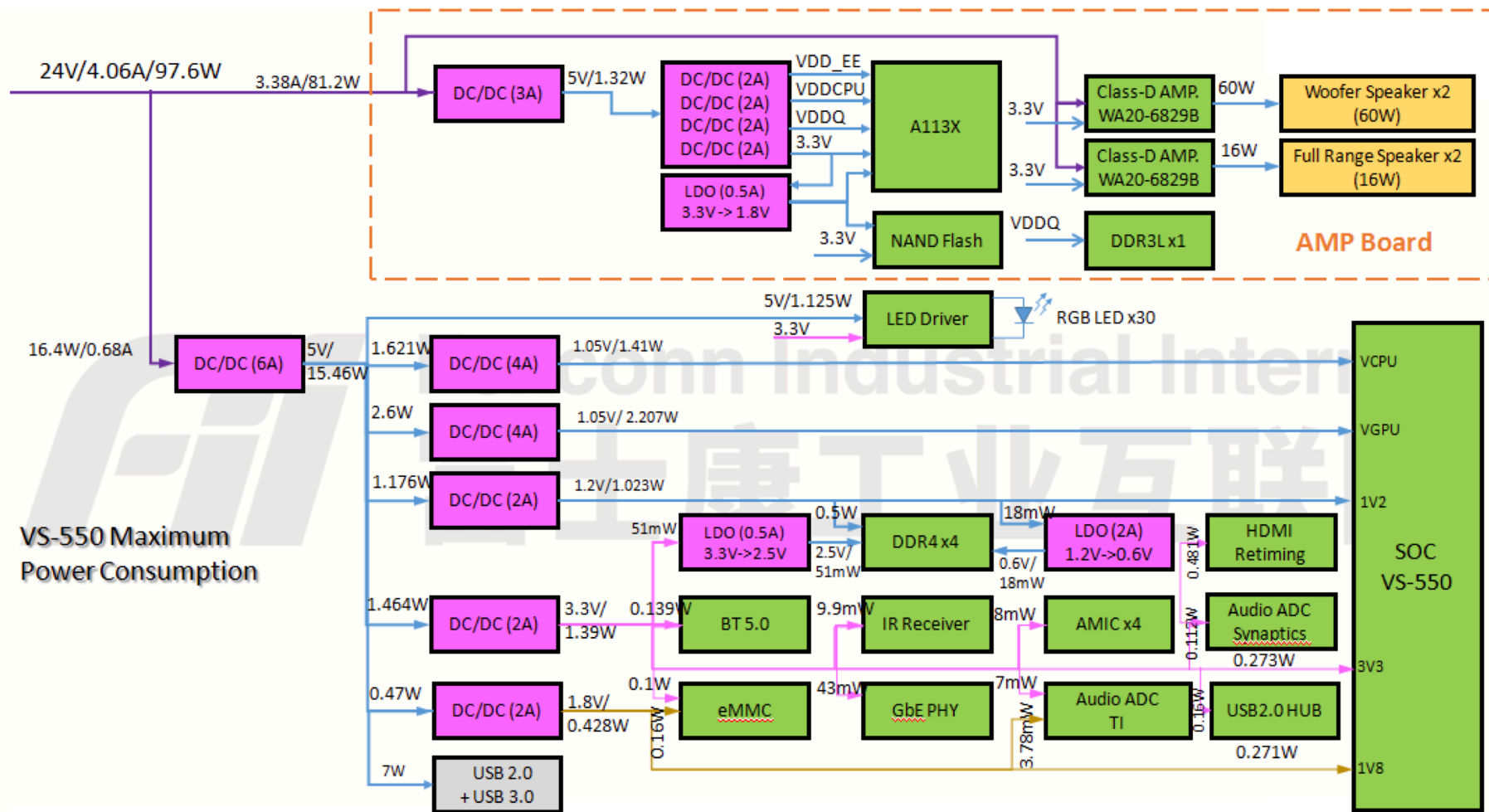
19: CONN - DEBUG
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BFX-UA300 System Block Diagram



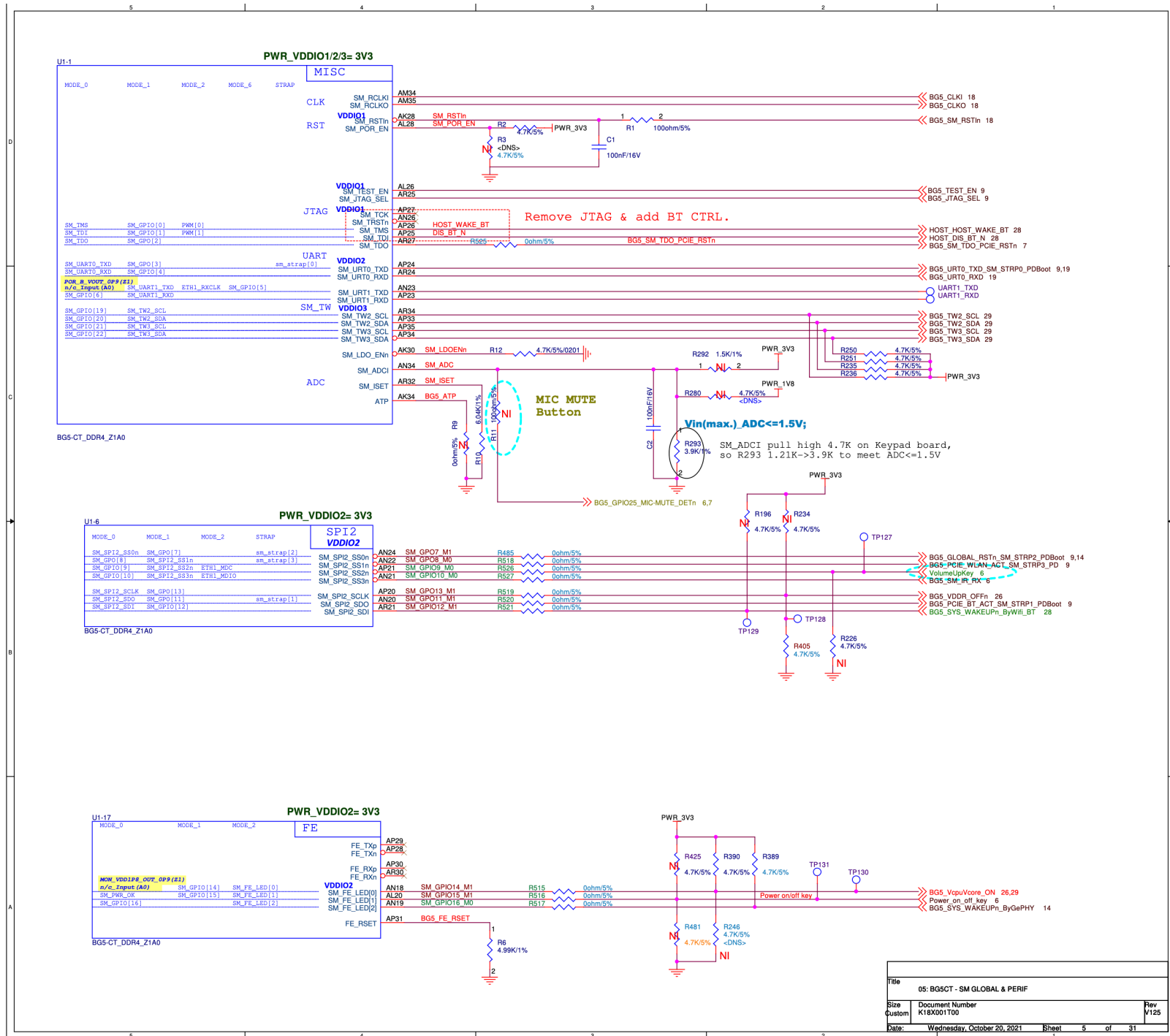
Title Block Diagram		
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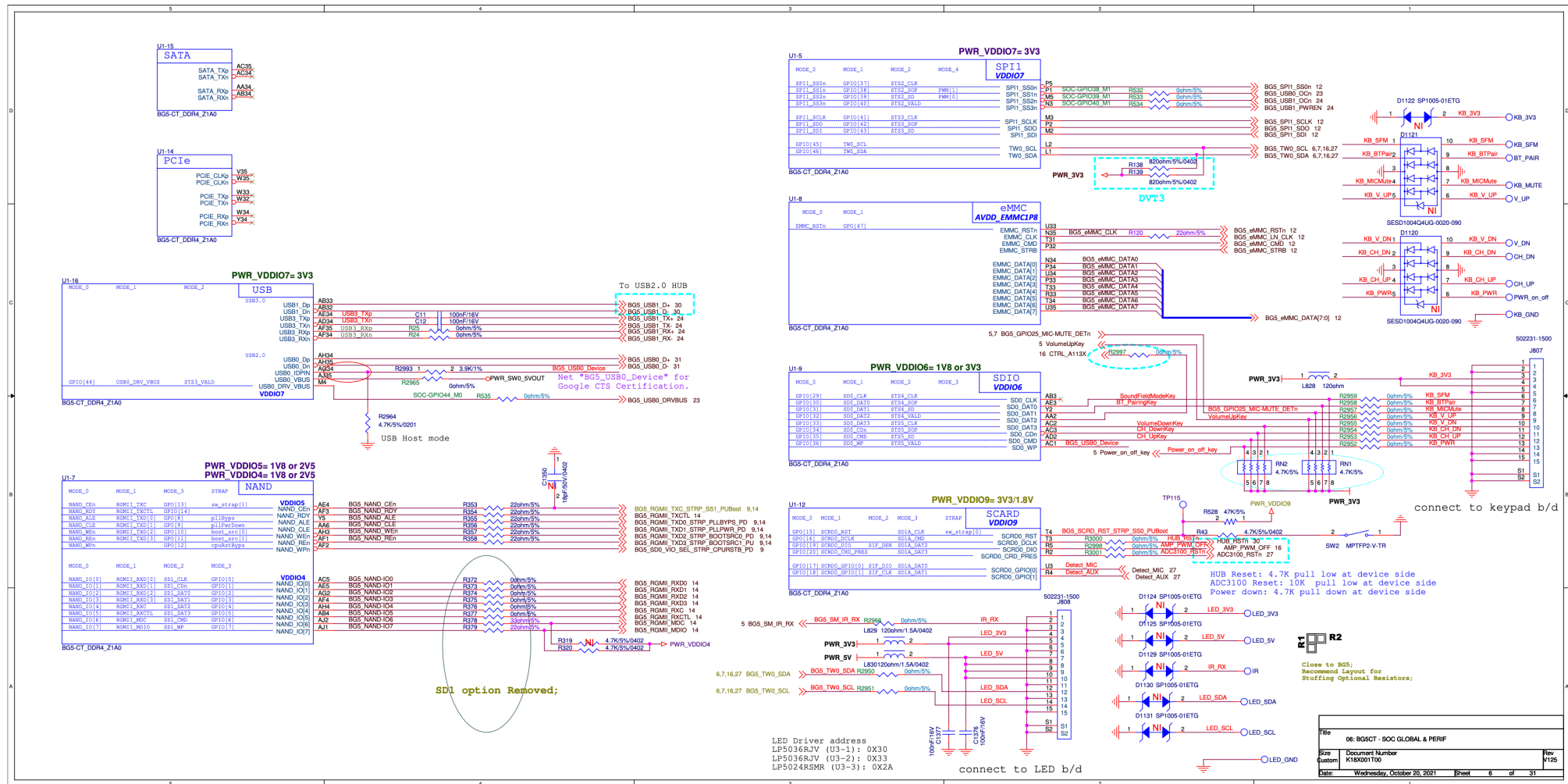


Title		
Power Tree		
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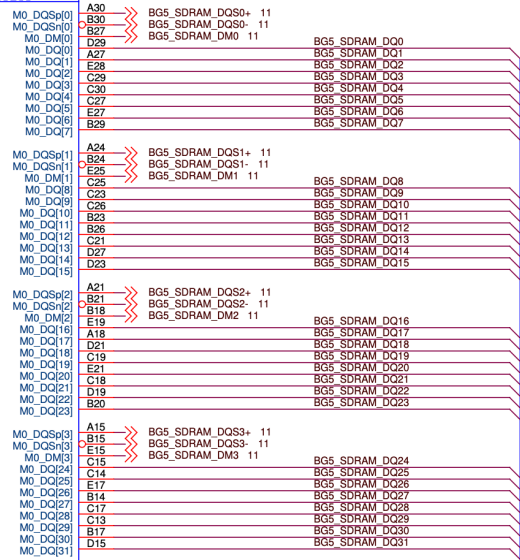
REVISION HISTORY

Version	Description
EVT1 00S0 (V005)	1. Add HL7593 circuit => U1323, C1454, C1455, C1449, C1450 for VCPU. 2. NI SY8824CAIC circuit => U68, C613, C614, R615 for VCPU. 3. Add HL7593 circuit => U1324, C1456, C1457, C1451, C1452 for VCORE. 4. NI SY8824CAIC circuit => U69, C623, C624, R626 for VCORE.



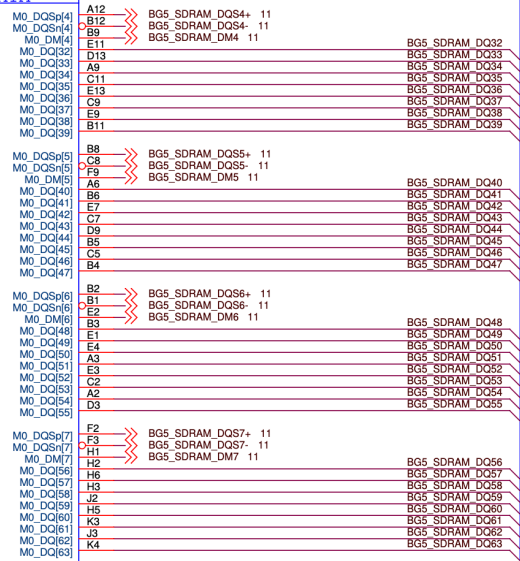


U1-3 DDR4 SDRAM - DATA



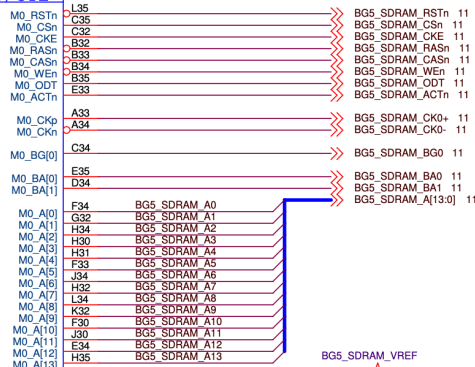
BG5-CT_DDR4_Z1A0

U1-4 DDR4 SDRAM - DATA

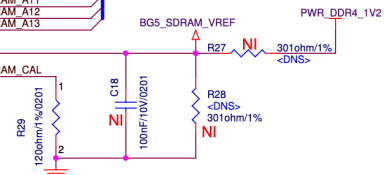


BG5-CT_DDR4_Z1A0

U1-2 DDR4 SDRAM - ADD/CTL

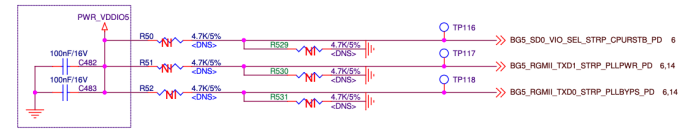
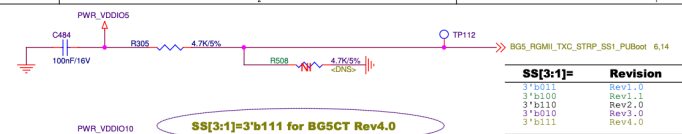


BG5-CT_DDR4_Z1A0

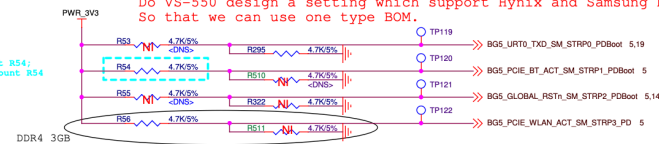


Title		
08: BG5CT - DDR4 PHY		
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S.No	Pad Name	Strap name in pinList	Description	Reg in global BIU	on-chip PUPD
1	SPOIF0	software_strap[2]	Straps for software usage	FRR_Gbl_ubootStrap_softwareStrap bit 2	N/A
2	I2S2_MCLK	software_strap[3]	Straps for software usage	FRR_Gbl_ubootStrap_softwareStrap bit 3	N/A
3	SCRD0_RST	software_strap[0](US B_BOOTn)	Straps for software usage ROM code will use this strap to decide booting from USB or not 0: Boot from USB	FRR_Gbl_ubootStrap_softwareStrap bit 0	PU
4	NAND_CEN	software_strap[1]	Straps for software usage	FRR_Gbl_ubootStrap_softwareStrap bit 1	PD
5	NAND_REn	boot_src[1]	CPU Boot Source bit[1]	FRR_Gbl_ubootStrap_bootSrc bit 1	N/A
6	NAND_WEn	boot_src[0]	CPU boot source bit[0] 00: ROM boot from SPI 01: NAND 10: ROM boot from EMMC 11: Direct boot from SPI(Only available when ENG_EN=1) When direct boot from SPI(SPI clear boot), pwrCntByps and cpuRstByps should be set to 1, plIByps Strap should be set to 0, plIPwrDown should be set to 0	FRR_Gbl_ubootStrap_bootSrc bit 0	N/A
7	NAND_WPn	cpuRstByps	CPU reset bypass strap 0: Enable reset logic inside cpu partition 1: Bypass reset logic inside cpu partition	FRR_Gbl_ubootStrap_cpuRstByps	PD
8	NAND_CLE	plIPwrDown	SYSTEM/CPU PLL Power Down 0: Power Down 1: Power UP	FRR_Gbl_ubootStrap_plIPwrDown	PD
9	NAND_ALE	plIByps	SYSTEM/CPU PLL Bypass indicator 0: No Bypass 1: All PLL Bypassed	FRR_Gbl_ubootStrap_sysPlIByps FRR_Gbl_ubootStrap_memPlIByps FRR_Gbl_ubootStrap_cpuPlIByps	PD
10	SM_URT0_TXD	SM_STRP[0]	SM to SOC RSTn mode select 0: SM_SOC_RSTOn_DO_FlModule releasing waits for SoCRstCnt but does not wait for SM_PWR_OK(mode_0 of SM_FE_LED[1] system will assert this signal when SOC core power is ready) 1: SM_SOC_RSTOn_DO_FlModule releasing waits for both SoCRstCnt and SM_PWR_OK		PD
11	SM_SPI2_SDO	SM_STRP[1]	software strap		PD
12	SM_SPI2_SS0n	SM_STRP[2]	software strap		PD
13	SM_SPI2_SS1n	SM_STRP[3]	software strap		PD

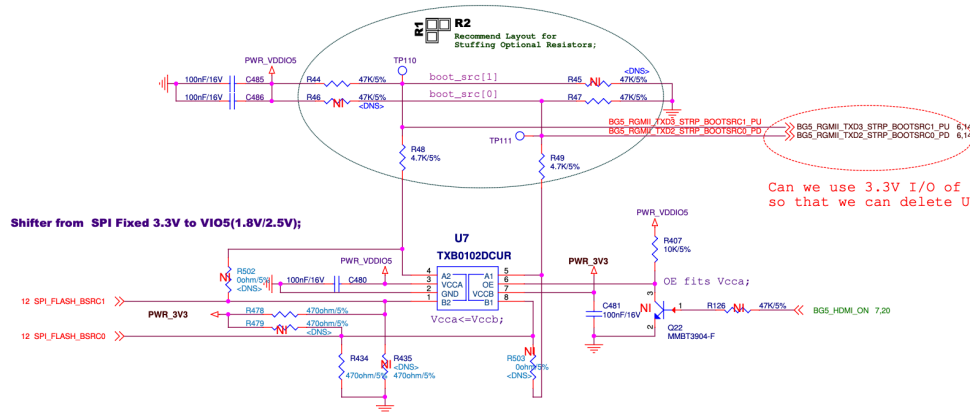


HL7593: mount R54;
8Y8824: no mount R54



Part Stuffing Guide for DDR Vendor on SM_STRP[3:1]

Vendor	SM_STRP [3]	SM_STRP [2]	SM_STRP [1]	Stuffed	Non-Stuffed
Hynix	0	Reserved	0	R511/R510	R54/R55/R56
Samsung	1	Reserved	0	R56/R510	R54/R55/R511
Micron	0	Reserved	1	R54/R511	R510/R55/R56
Reserved	1	Reserved	1	R54/R56	R511/R55/R510

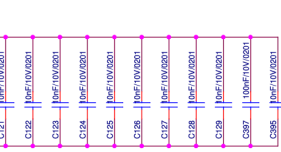
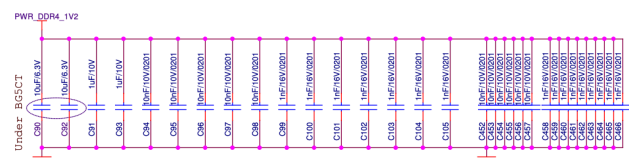
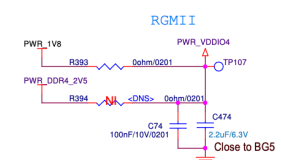
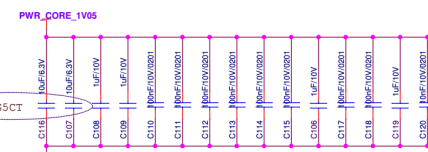
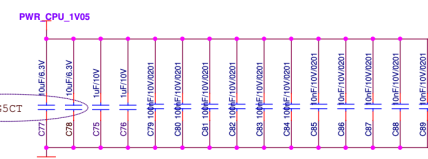
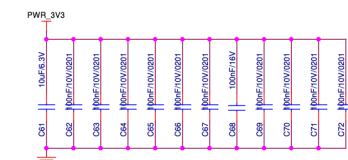
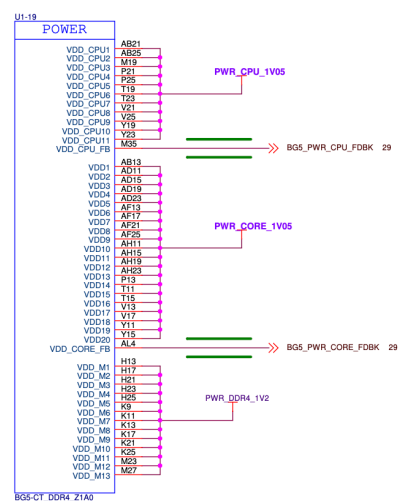
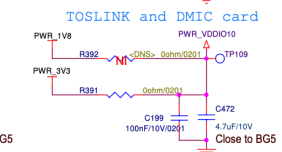
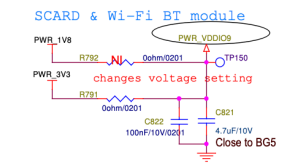
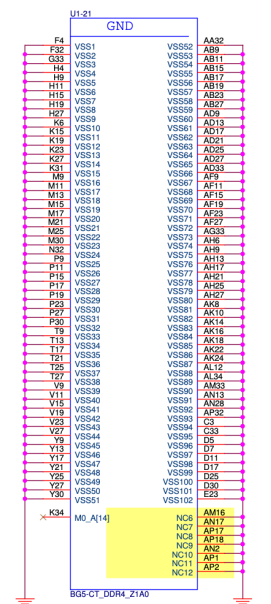
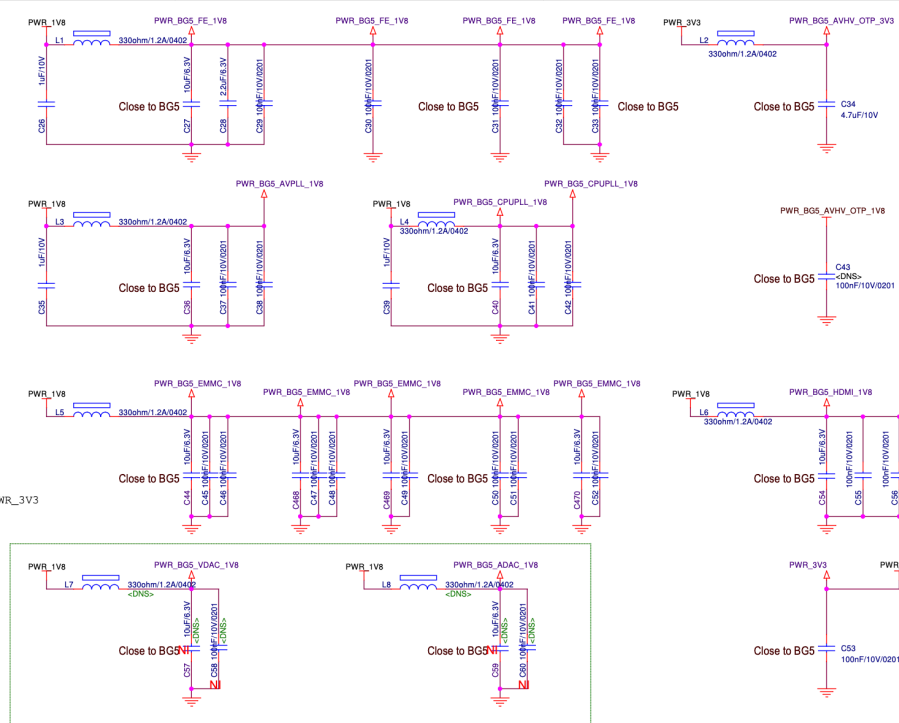


File	09: BG5CT - PIN STRAP
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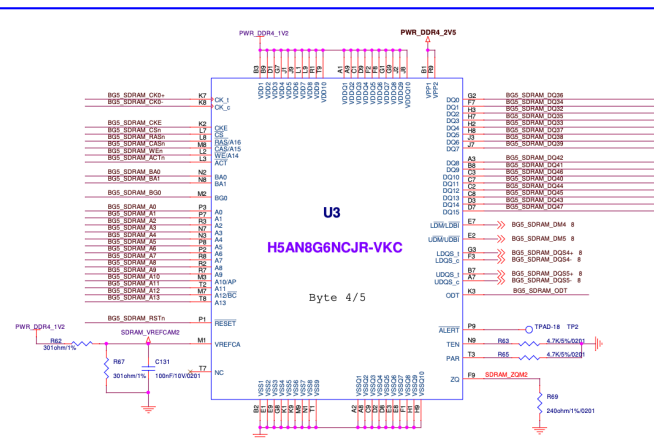
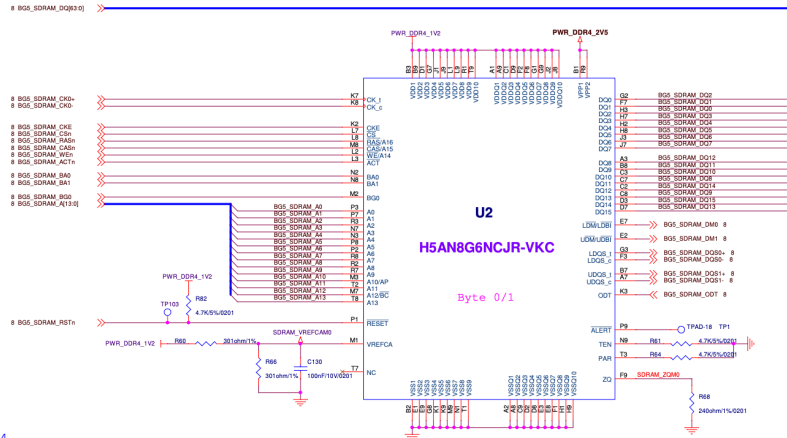
PWR_VDDIO6 connected to PWR_3V.

VDDIOx Vs Signal Allocation

VDDIO1	= SM: PRT_EN, RST, JTAG
VDDIO2	= SM: URT0/1, SPI2, FE_LED, HPD/CCEC
VDDIO3	= SM: TWSI2/3
VDDIO4	= NAND, SDIO1, RGMII
VDDIO5	= NAND, RGMII
VDDIO6	= SDIO0
VDDIO7	= SPI1, TWSI0
VDDIO8	= STS0/1
VDDIO9	= SCDR, SD1A
VDDIO10	= I2S1/2, SPDIFO, STS6/7, SD1B
VDDIO11	= DDC

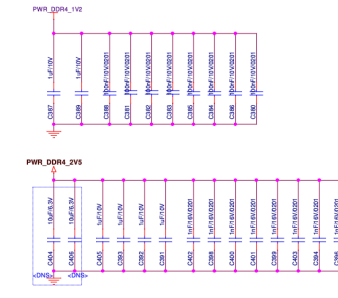
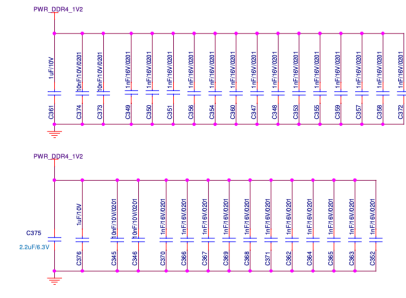
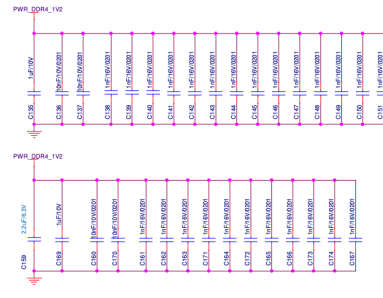
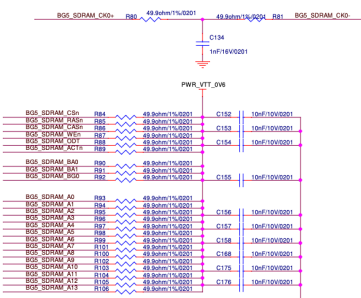
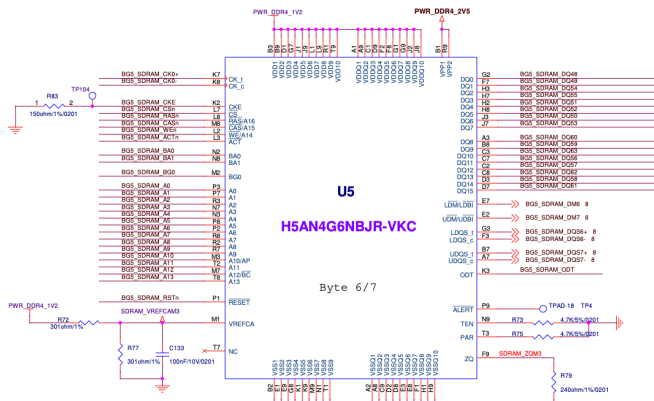
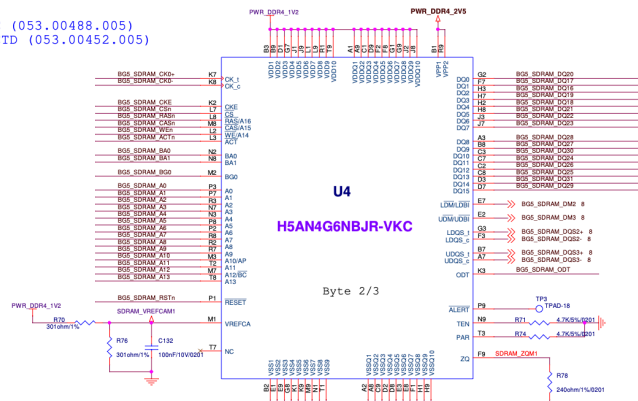


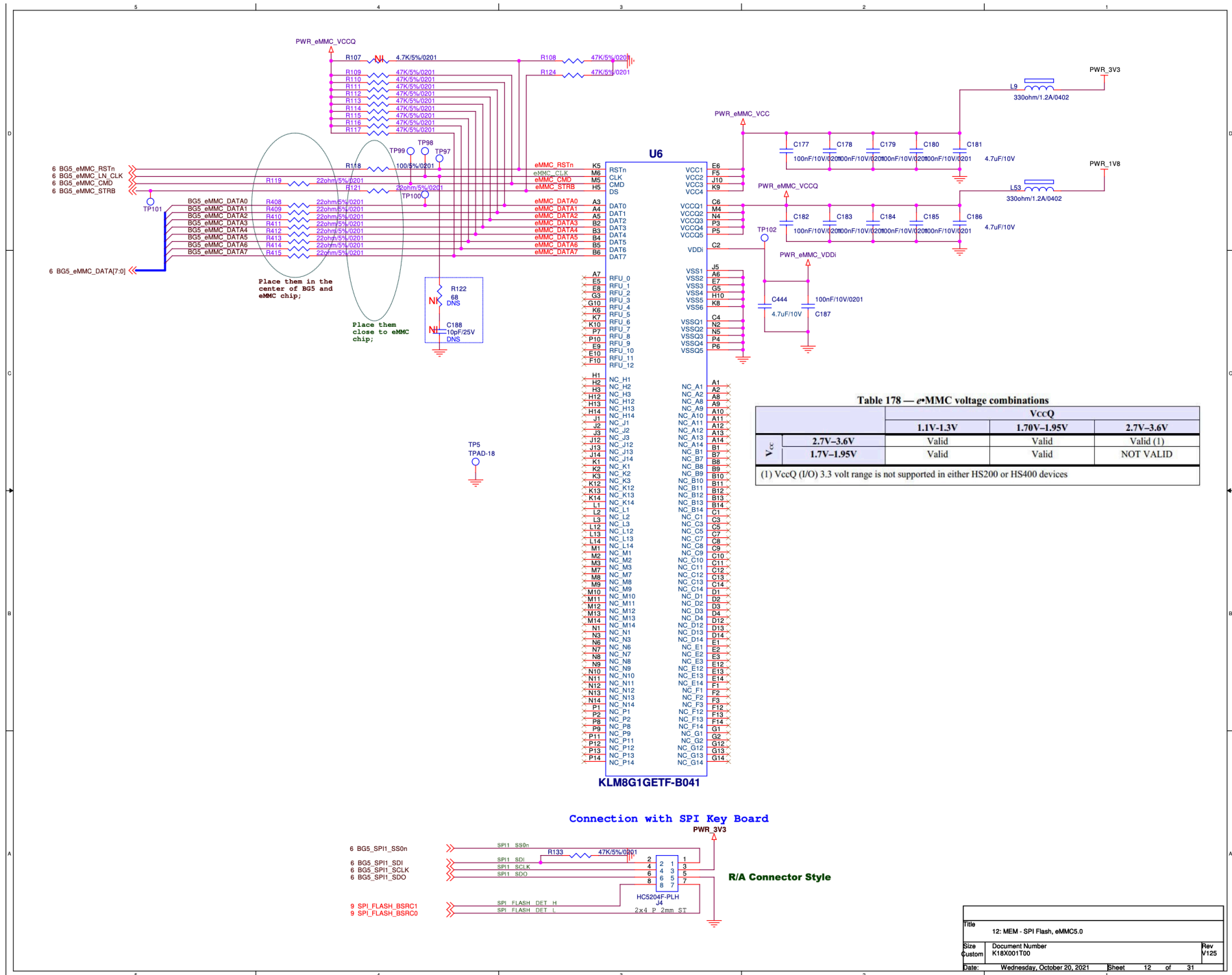
Delete U13 uSD card power

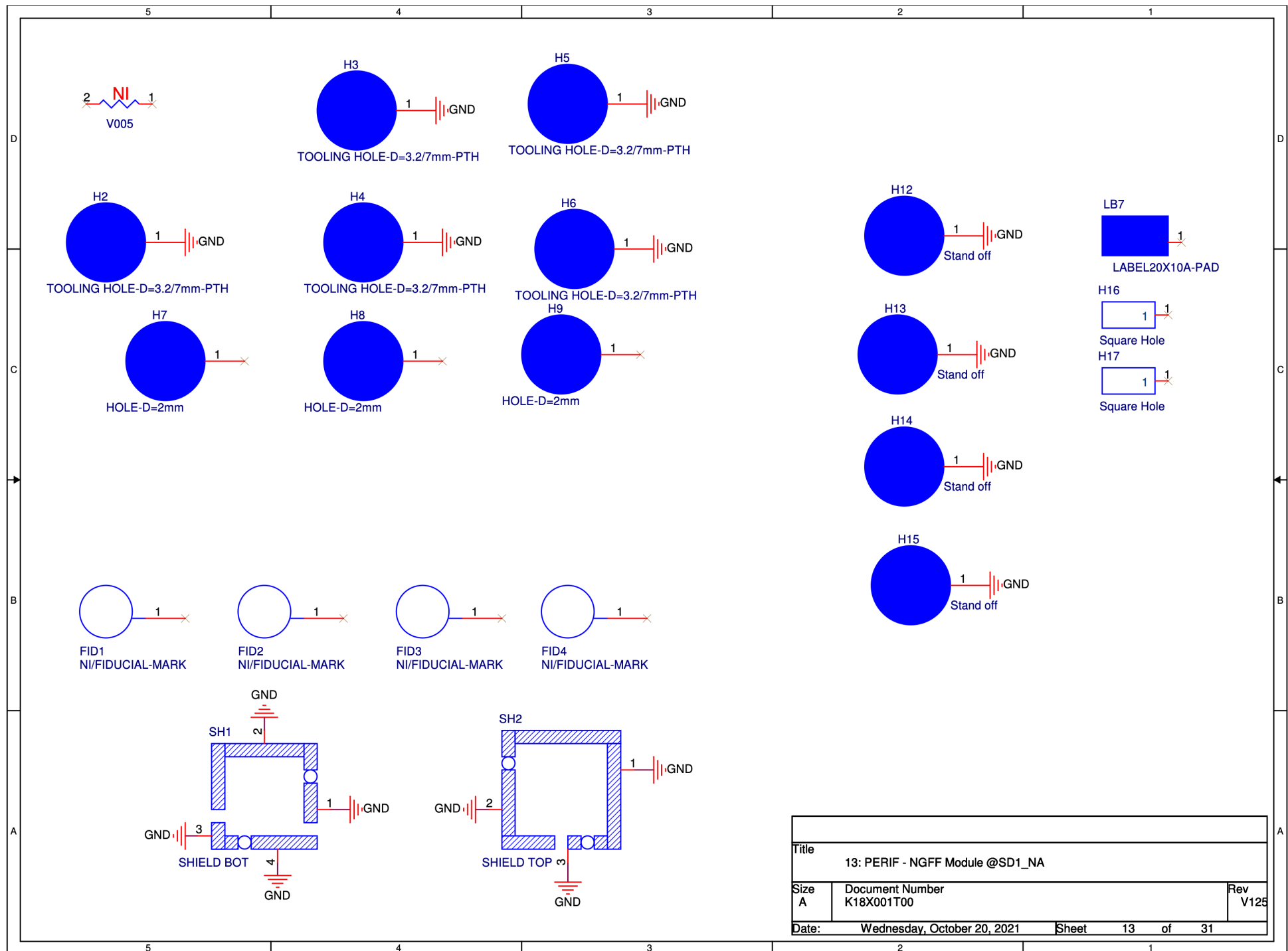


4Gb DDR4
1. Hynix: H5AN4G6NBJR-VKC (053.00495.005)
2. Samsung: K4A4G165WF-BCTD (053.00474.005)

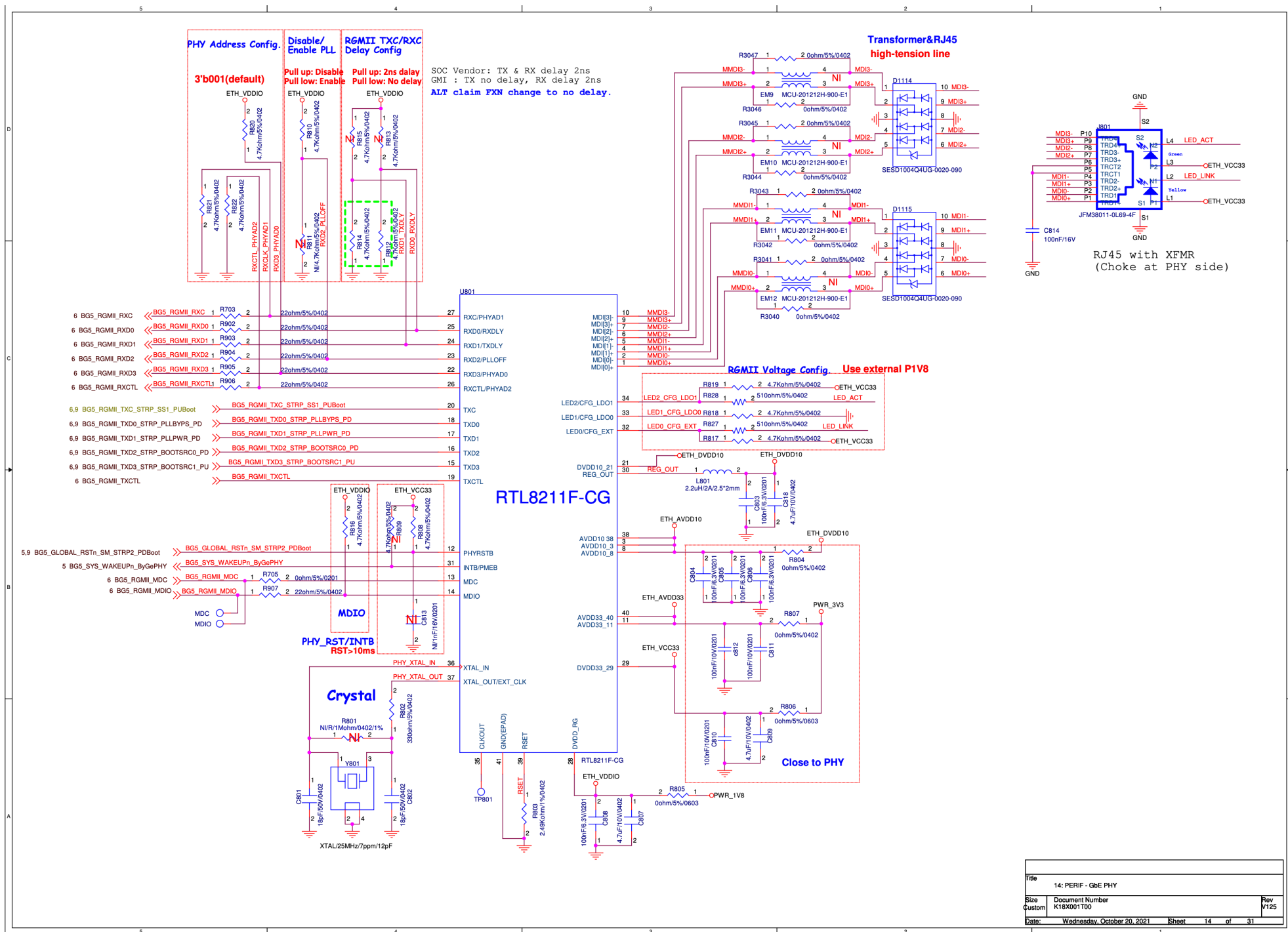
8Gb DDR4
1. Hynix: H5AN8G6NCJR-VKC (053.00488.005)
2. Samsung: K4A8G165WC-BCTD (053.00452.005)





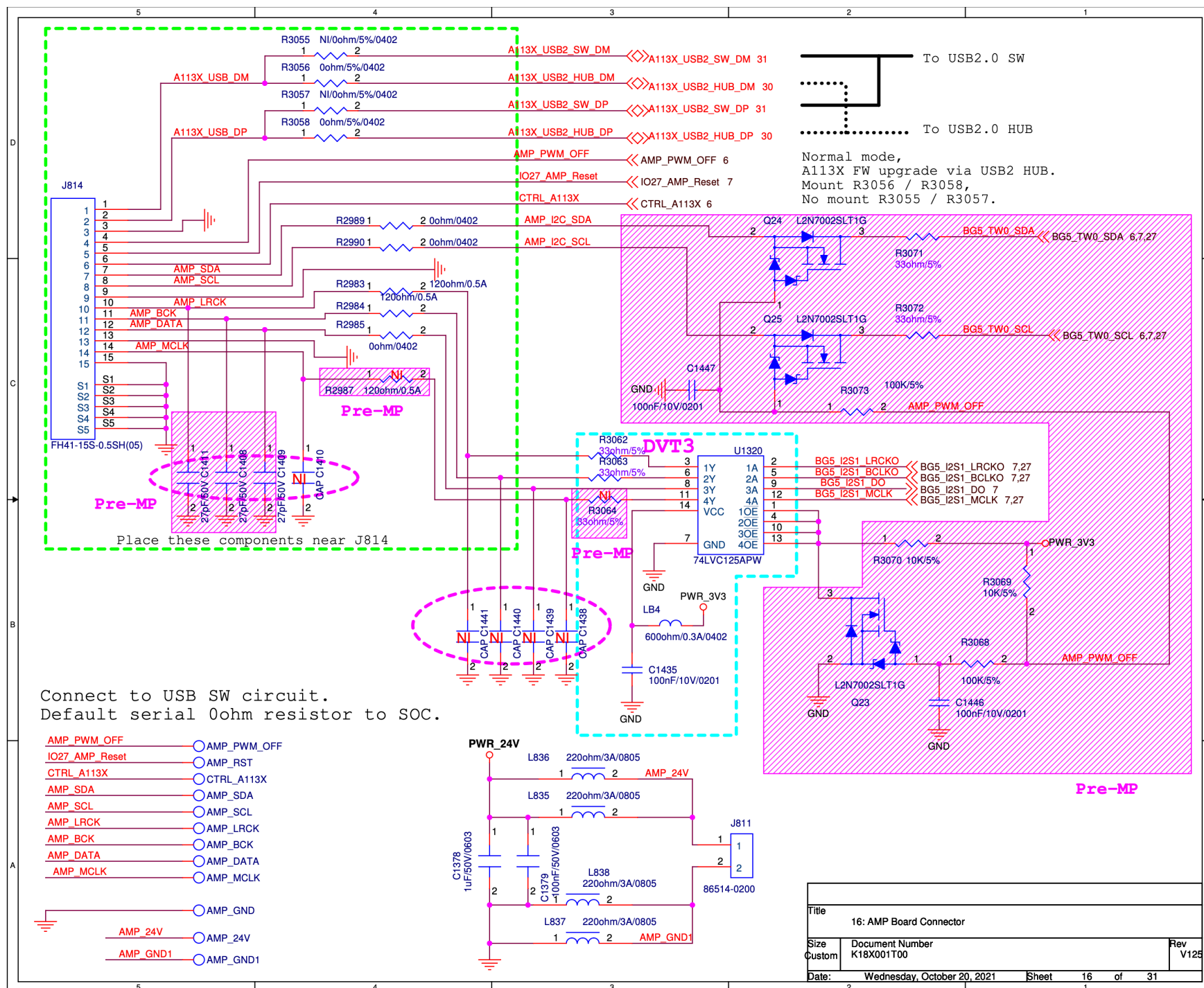


Title		
13: PERIF - NGFF Module @SD1_NA		
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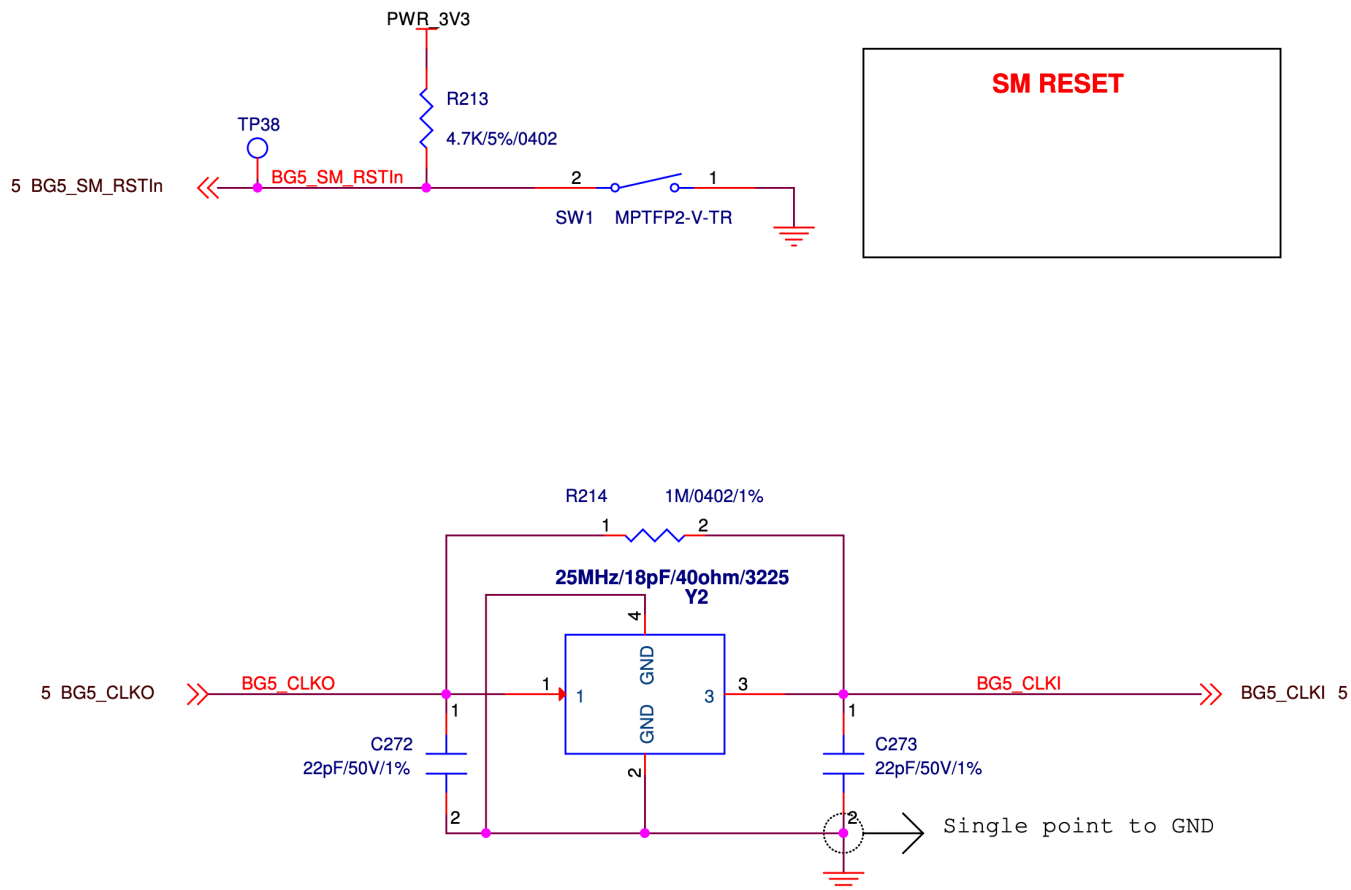
Delete CX20921-21Z circuit

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15: PERIF - Voice Processor_NA			
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Delete Smart card and TOSLINK circuit

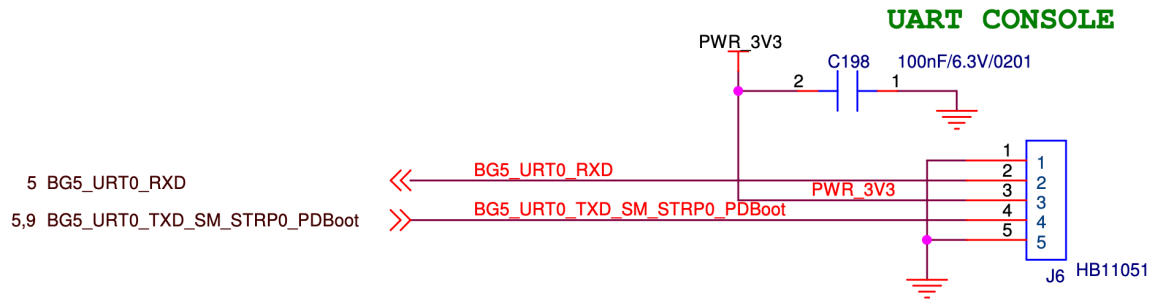
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17: PERIF - SPDIF TX, TSI IF_NA		
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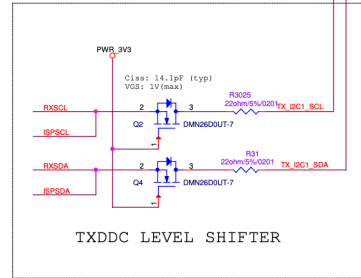
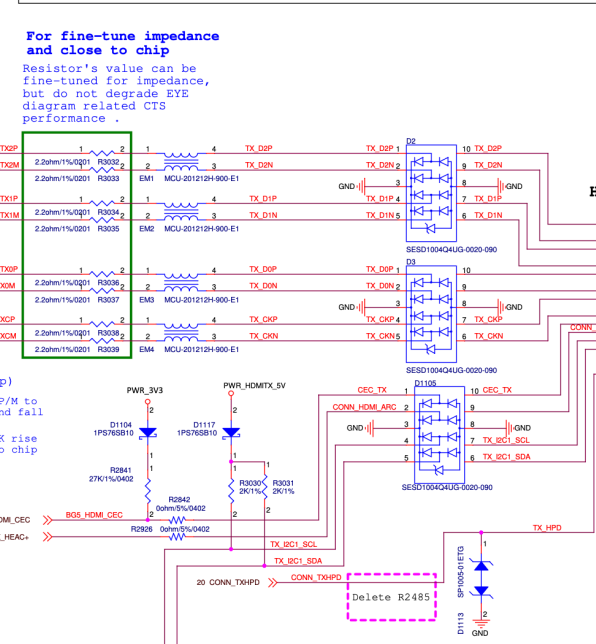
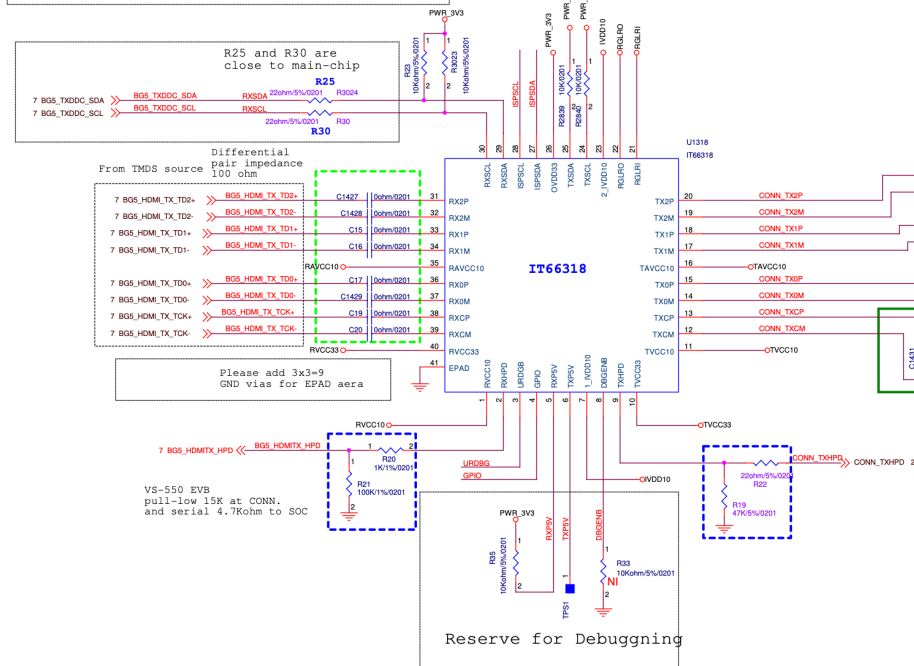
Changes IR receiver to LED board.

Title		
18: PERIF - RST, CLKGEN & IR IN		
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Delete J5 JTAG CONN.
Delete J20 CVBS and audio header
Delete FMJ01 BMJ02
for MIC card and Digital audio I2S header



Title		
19: CONN - DEBUG		
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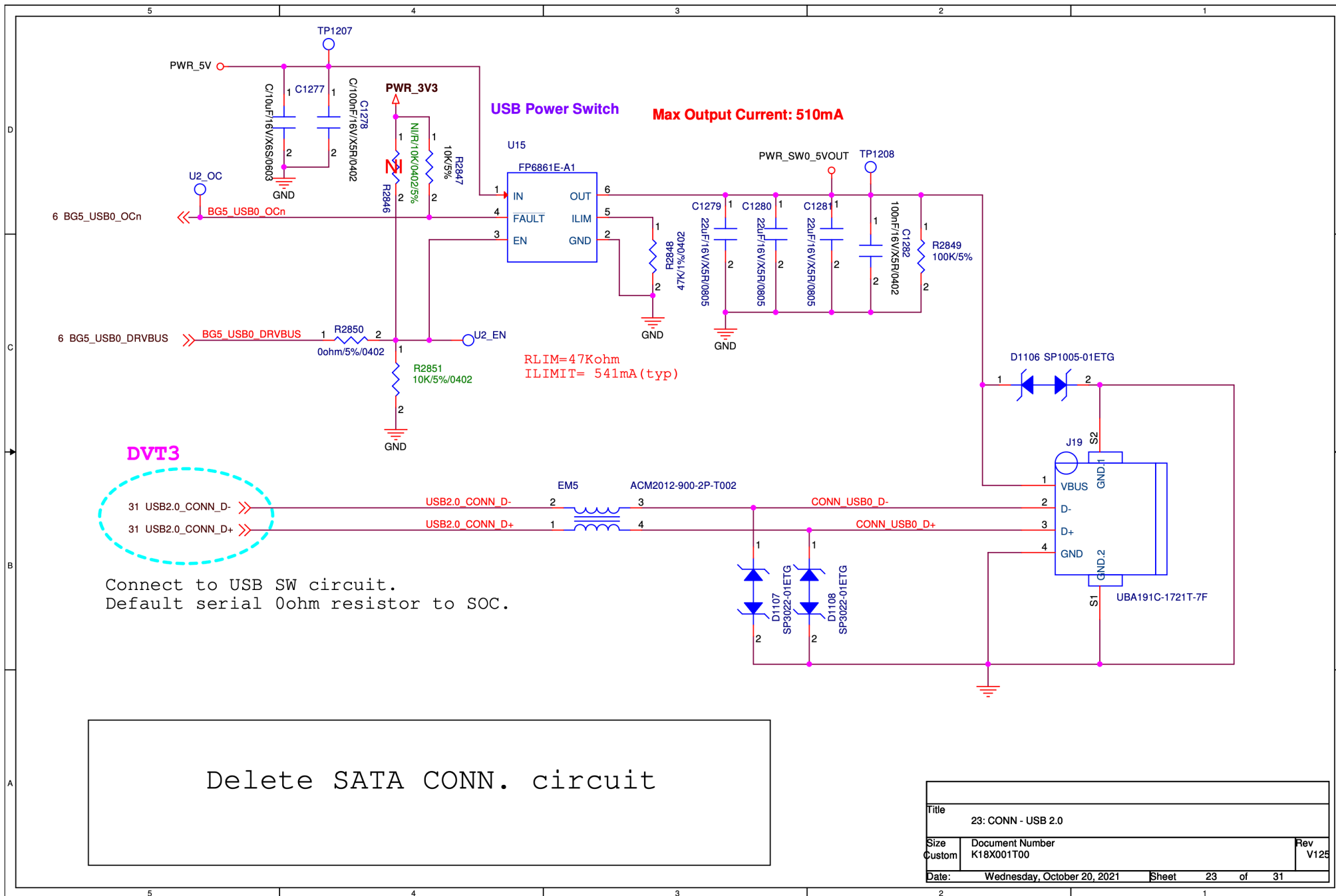
Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

5					4					3					2					1																																																																																																								
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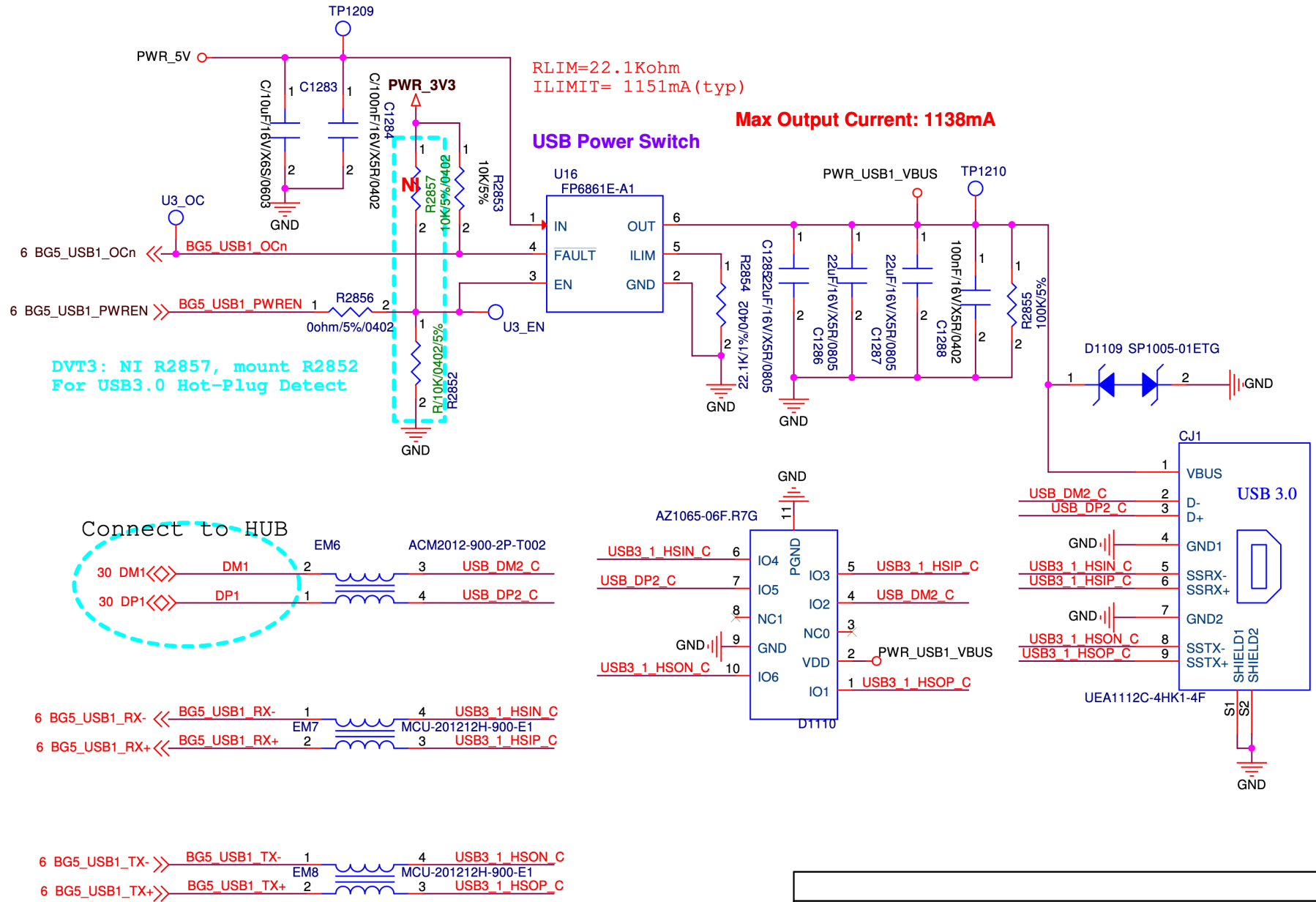
Title 21: CONN -MicroSD Socket@SD0_NA									
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Delete PCIe and J18 (Smart card) card circuit

Title		
22: CONN - Mini PCIe_NA		
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23: CONN - USB 2.0		
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24: CONN - USB 3.0		
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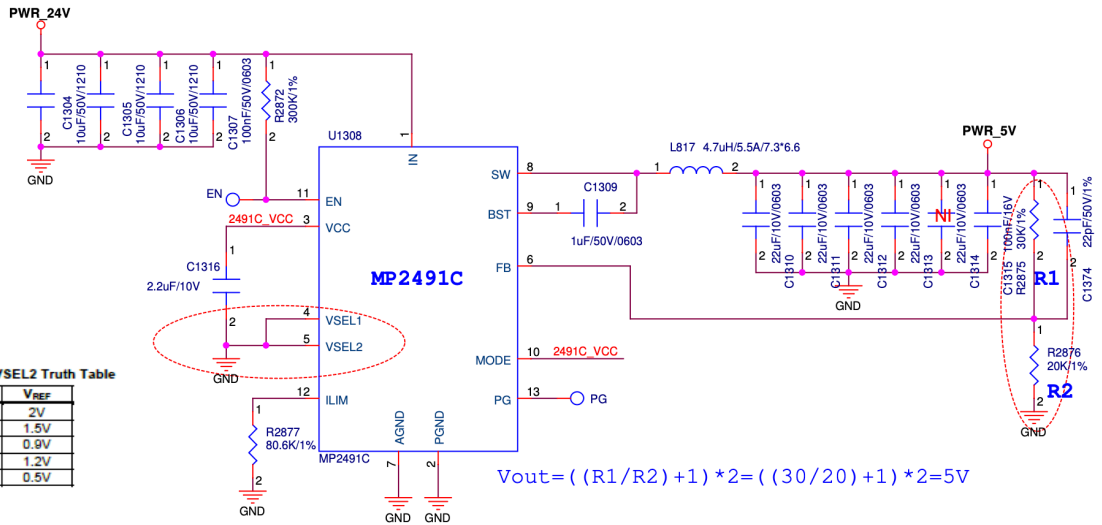
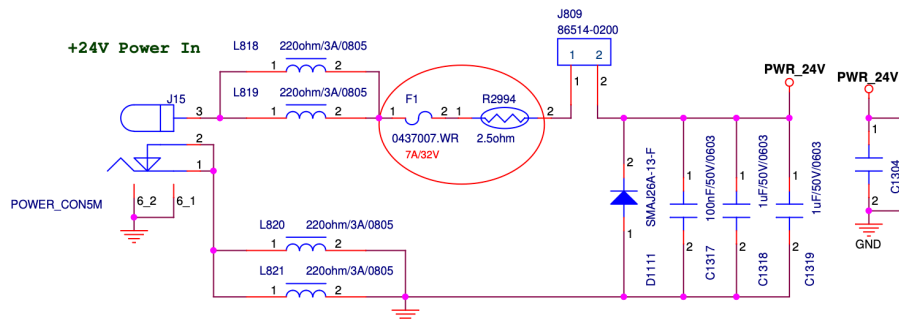
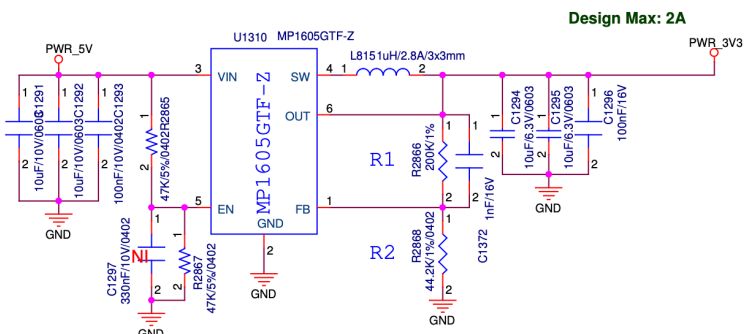


Table 2: VSEL1, VSEL2 Truth Table

VSEL1	VSEL2	V _{REF}
0	0	2V
VCC	0	1.5V
0	VCC	0.9V
1/2*VCC	0	1.2V
VCC	VCC	0.5V

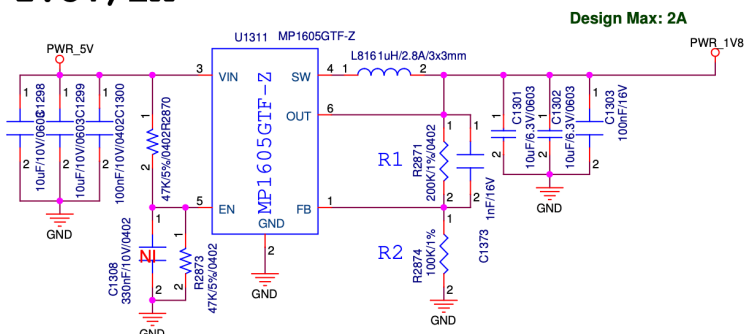
$$V_{out} = ((R1/R2) + 1) * 2 = ((30/20) + 1) * 2 = 5V$$

3.3V/2A



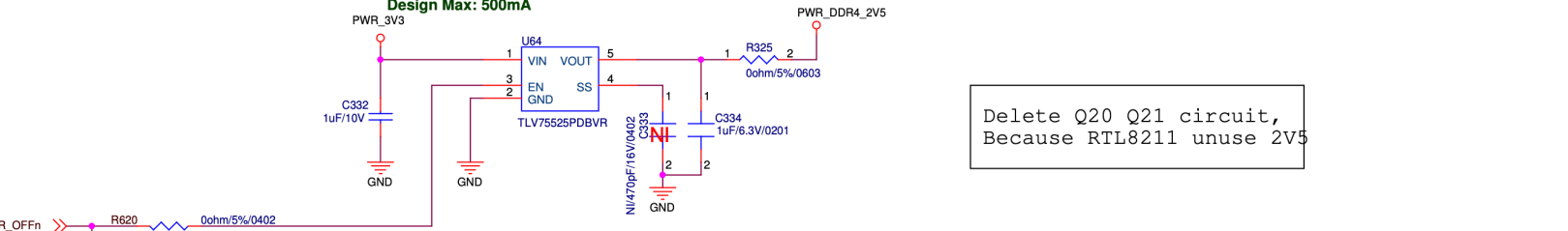
$$V_{out} = ((R1/R2) + 1) * 0.6 = ((200/44.2) + 1) * 0.6 = 3.315V$$

1.8V/2A

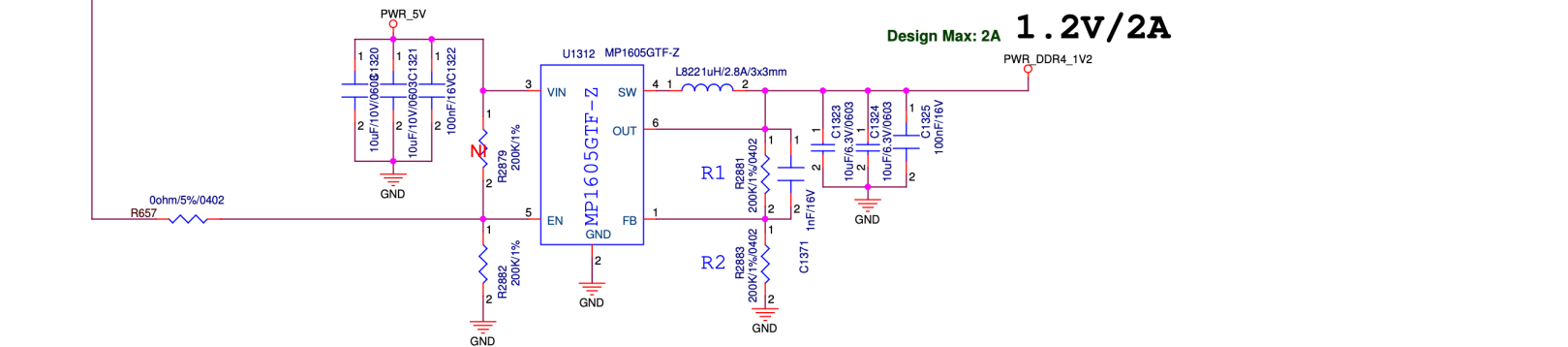


$$V_{out} = ((R1/R2) + 1) * 0.6 = ((200/100) + 1) * 0.6 = 1.8V$$

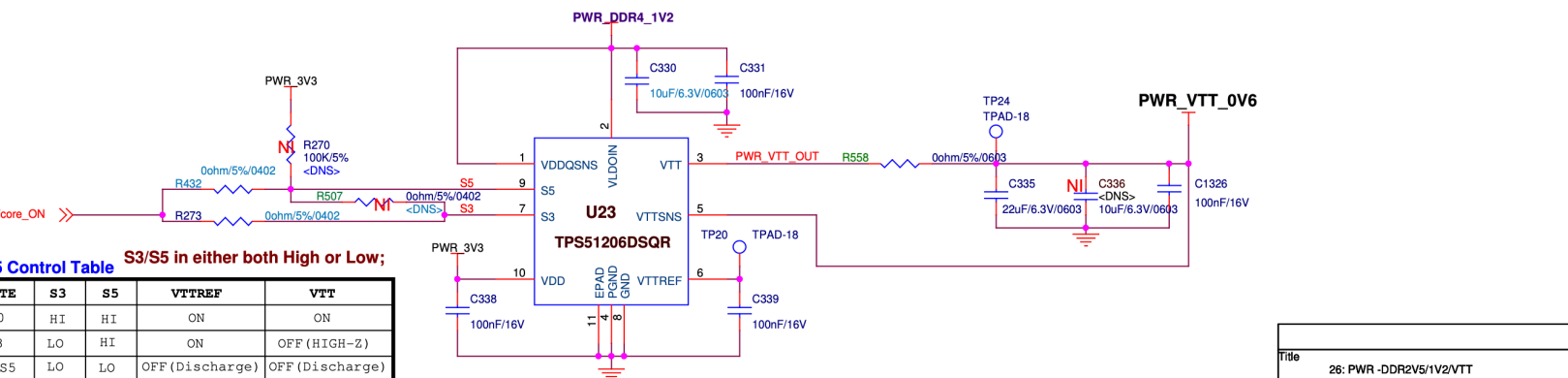
Title		
25: PWR -3V3/1V8		
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Delete Q20 Q21 circuit,
Because RTL8211 unuse 2V5

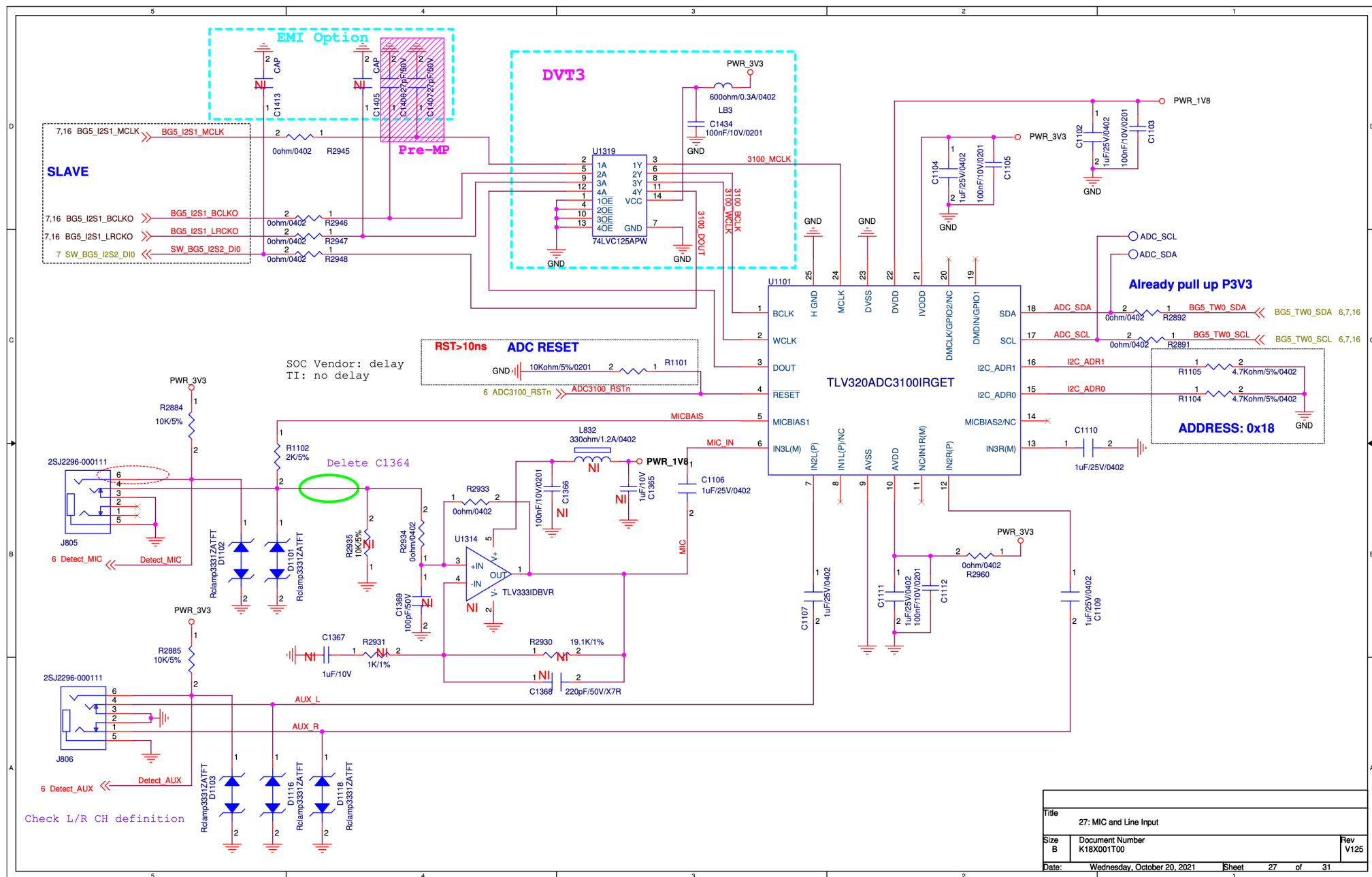


$$V_{out} = (R_1/R_2 + 1) * 0.6 = ((200/200) + 1) * 0.6 = 1.2V$$



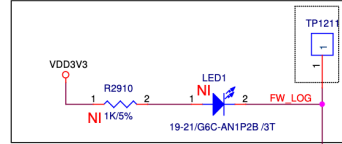
S3/S5 Control Table **S3/S5 in either both High or Low;**

STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF (HIGH-Z)
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)



Recommended LED function connection

Note:
If SPS mode, then R33 10 kohm pull-low, R32 NC and L4 2.2 uH.
If LDO mode, then R33 NC, R32 10 kohm pull-high and L4 0 ohm.

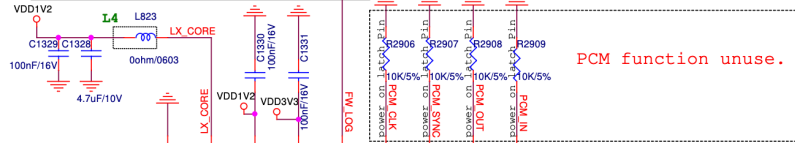


Note:
Pin 29 LED[0] is FW debug log pin,
must be placed the jumper or test point for debug.

Optional connection to HOST

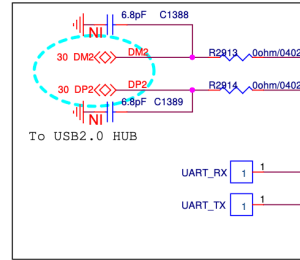
Note:
WLAN_ACT: Reserved interface for RTK, it could be used as GPIO, add a 10 kohm resistor pull low to GND.

Note:
3.3 V power pin recommended cap type is X5R/10V or above.
1.2 V power pin recommended cap type is X5R/6.3V or above.
RF power pin (Pin 13, 14, 16 & 17) cap value can not be less than 1 uF.



PCM function unused.

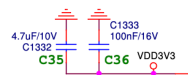
BQB certification interface



Note:
I2C_SCL & I2C_SDA are BQB Uart for BQB certification.

Must be placed reserved test points and could be disconnected with host module for BQB certification by 0 ohm resistor.

C35 (4.7 uF) -> C36 (0.1 uF) -> Pin1 placing order in PCB layout



RTL8761BUV QFN32

Optional connection to HOST

	I/O Type	Active	Normal
PIN10 HOST_WAKE_BT	IN		
PIN11 BT_WAKE_HOST	OUT	High	Low
PIN12 DIS_BT_N (Reset)	IN	Low	High

BQB Uart_In BQB Uart_Out

Note:
BT_WAKE_HOST is "EEPROM_SEL" power on latch pin.
Must be placed the pull-low 10 kohm resistor to GND.

Note:
"DIS_BT_N" pin could be connected to the host to implement reset function.

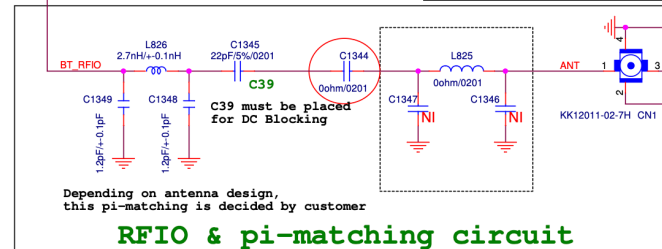
Note:
BT_ACT is "SPS_LDO_SEL" power on latch pin
Selection of 1.2V Power Supply Mode:
1.If SPS mode is selected, a 10 kohm is placed to connected to GND. L4 should be placed 2.2 uH.
2.If LDO mode is selected, a 10 kohm is placed to connected to VDD3V3. L4 should be placed 0 ohm.

Note:
BT_STE is "TEST_MODE_SEL" power on latch pin.
Must be placed the pull-low 10 kohm resistor to GND.

Note:
BT_VD12SYN power pin must be placed 1 uF and C50 (for adjustment) capacitors in parallel.

Note:
1. The spec of 40 Mhz xtal is with recommended loading cap 9 pF.
2. The loading capacitance is implemented in RTL8761BUV IC, C34 & C36 could be NC but must be placed for reservation.

40 MHz xtal clock

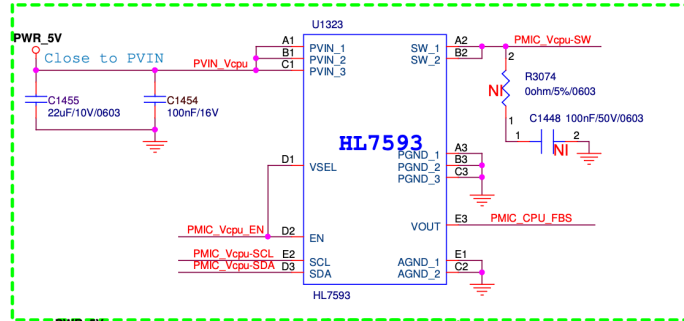


Depending on antenna design,
this pi-matching is decided by customer

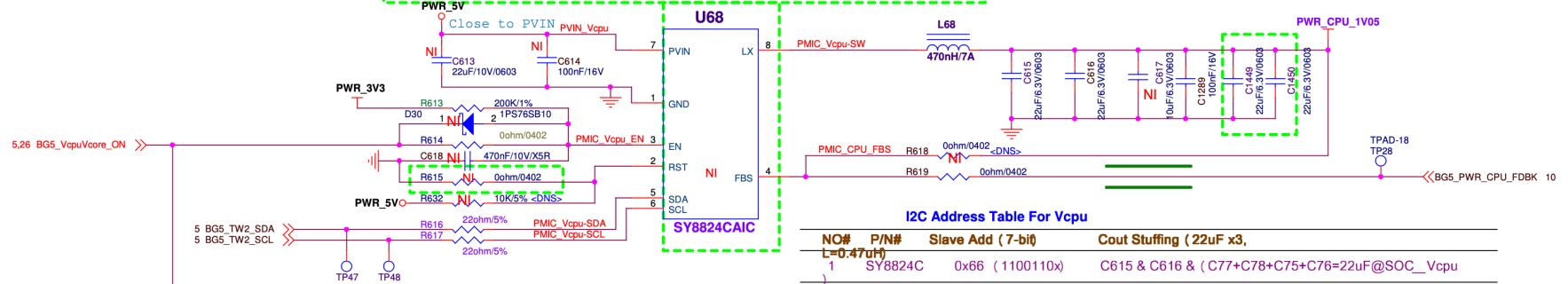
RFIO & pi-matching circuit

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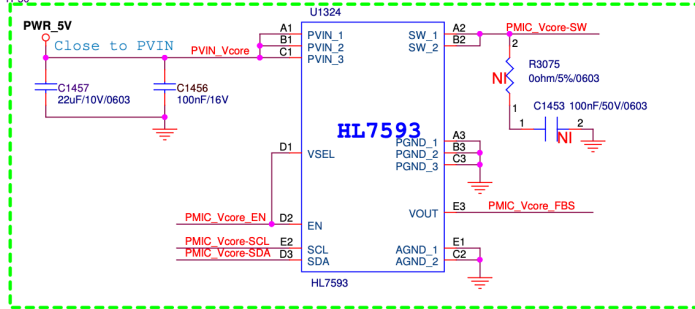
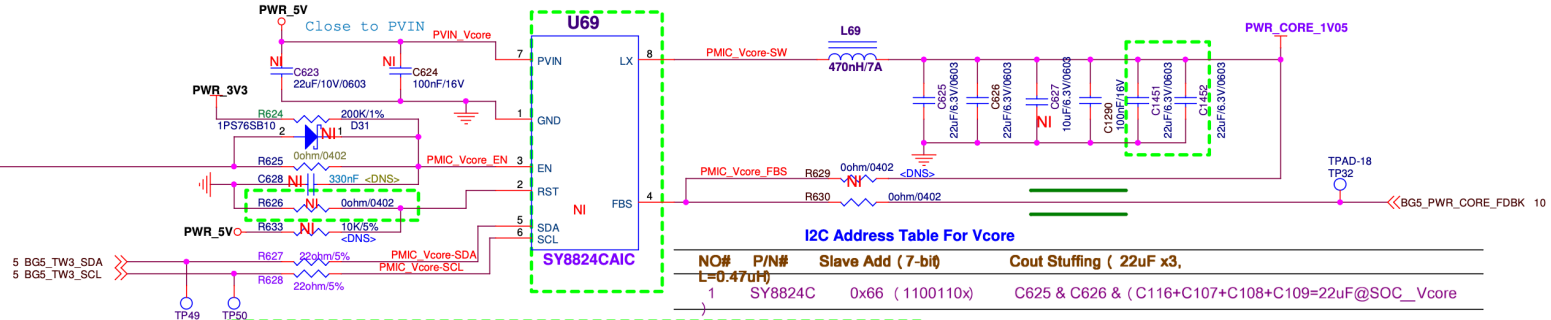
Default 1.05V/4A for Vcpu;



	C1454,C1455 C1456,C1457 C1449,C1450 C1451,C1452	C613,C614 C623,C624	R615,R620
SY8824	No mount	Mount	Mount
HL7593	Mount	No mount	No mount



Default 1.05V/4A for Vcore;



Title			
29: Power Vopu Vgpu			
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